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METHOD AND APPARATUS FOR SHARING SIGNAL PINS ON AN INTERFACE BETWEEN A SYSTEM CONTROLLER AND PERIPHERAL INTEGRATED CIRCUITS

BACKGROUND OF THE INVENTION

1.   Technical Field:

The present invention relates generally to interface signaling, and more particularly, to an interface between a system controller integrated circuit and a plurality of peripheral integrated circuits.

2.   Description of the Related Art:

Interfaces between present-day integrated circuits have increased in density and variety. In particular, computer systems peripheral components have interfaces that differ based upon the type of peripheral, and all of the peripheral components may have many connections.

Typically, the width of an address and data bus for interconnecting peripheral components to a system controller is determined by the maximum number of address signals and the maximum number of data signals. The width of a control bus may depend upon the variety of control mechanisms used to interface the various peripheral integrated circuits. For example, a memory device may require a read/write line and a strobe line, while an Input/Output (I/O) controller may require a read strobe and a write strobe. Therefore, the total number of interface signals for connection to a group of peripheral

devices generally reaches the maximum data and address set
plus a variety of control signals that includes all of the
required "flavors", plus a plurality of chip select
signals for selecting between the particular peripheral
integrated circuits.

Since the above signals have different setup and
timing requirements, it is not practical for the logic
that generates these signals to shift functions between
the functions required for the various peripherals, for
example, a memory IC requiring 16 address lines sets a
minimum number of address lines in a typical interface to
16. A secondary connection of a bus controller that
requires only 5 address lines leaves 11 of the address
lines provided on the interface unused for the purposes of
interfacing the bus controller. Further for example, if
the bus controller requires 6 high-speed control lines and
the memory IC requires only 2, but of completely differing
types, 8 control signal lines must be provided on the
interface. The above design yields 13 unused signal lines
during interfaces to the bus controller and 6 unused
control lines during interfaces to the memory.

It is therefore desirable to provide a method and
apparatus for sharing pins between disparate signals on an
interface to a plurality of peripheral integrated
circuits.

SUMMARY OF THE INVENTION

The objective of sharing an interface pin between disparate signals is accomplished in a method and apparatus for interfacing a system controller integrated circuit and a plurality of peripheral integrated circuits. The interface circuit shares an interface pin by selecting between circuits for communicating with each of the peripheral integrated circuits. The selection is made by a signal within the system controller integrated circuit that provides sufficient setup and hold times for signals on the interface pin such that they are consistent with the setup and hold time requirements of the peripheral integrated circuits.

The foregoing and other objectives, features, and advantages of the invention will be apparent from the following, more particular, description of the preferred embodiment of the invention, as illustrated in the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the
invention are set forth in the appended claims. The
invention itself, however, as well as a preferred mode of
use, further objectives, and advantages thereof, will best
be understood by reference to the following detailed
description of an illustrative embodiment when read in
conjunction with the accompanying drawings, wherein like
reference numerals indicate like components, and:

Figure 1 is a block diagram of an interface in
accordance with a preferred embodiment of the invention.

Figure 2 is a schematic diagram of a system
controller interface circuit with a preferred embodiment
of the invention.

Figures 3A-3D are schematic diagrams of selection
circuits in accordance with various embodiments of the
invention.

Figure 4 is a timing diagram depicting signals within
the interface of Figure 1.

DESCRIPTION OF ILLUSTRATIVE EMBODIMENT

With reference now to the figures, and in particular
with reference to **Figure 1**, there is depicted a block
diagram of an interface **10** in accordance with an
embodiment of the invention. A system controller
integrated circuit provides an interface **10** for connection
to a plurality of peripheral integrated circuits, which
may include memories or other system components. In the
exemplary embodiment, the peripheral integrated circuits
include a peripheral controller integrated circuit **14** and
a memory **16**. Peripheral integrated circuit **14** and memory
16 share peripheral interface signals **18**, and in contrast
to the prior art, the shared signals **18** include common
connections of at least one shared pin on system
controller integrated circuit **12** to pins of differing
signal types on peripheral integrated circuit **14** and
memory **16**. The exemplary embodiment depicts two peripheral
components, but in practice the number of peripheral
components sharing pins via shared interface signals **18**
will be dictated by particular design requirements and
fan-out capabilities.

Peripheral integrated circuit **14** may be of various
types, for example, a Personal Computer Memory Card
International Association (PCMCIA) bus controller, other
bus controller or a direct peripheral control device such
as a Integrated Drive Electronics (IDE) controller. The
one requirement for the application of the interface
circuits of the present invention is that all of the
peripheral integrated circuits (including memories such as
memory **16** or other devices) sharing an interface pin have
a chip-select mechanism whereby the shared interface

signal connections **18** to peripheral integrated circuits
are isolated from those circuits that are not selected.
The isolation means that unselected peripherals will not
generate any activity on the shared signals or react via
internal state changes to variations on the shared
signals. Interface **10** may include unshared signals **15A**
and **15B** depending on system requirements.

Referring now to **Figure 2**, details of system
controller integrated circuit **12** in accordance with an
embodiment of the invention are depicted. Internal to
system controller integrated circuit **12**, signals are
generated for interface to peripheral A and peripheral B
and are coupled to a selection circuit **24** for selecting
between the signals for output to a shared interface
signal **18**. The select input of selection circuit **24** is
coupled to an internally generated peripheral select
signal **SEL A/B** provided by a chip select control circuit
22. Select signal **SEL A/B** is a signal used by chip select
control circuit **22** to generate the actual chip select
signals **/CS1** and **/CS2** and has leading-edge timing
sufficient advanced from the chip select signals so that
selection circuit **24** (which includes the pin driver for
the shared interface signal if the shared interface signal
is an output) can provide the proper signal to the shared
interface pin for the peripheral to be selected. Further,
select signal **SEL A/B** must remain valid after the trailing
edges of the chip select signals so that the proper signal
is maintained on the shared interface pin to meet the hold
time requirements of all of the peripheral integrated
circuits. While the exemplary embodiment depicted in
Figure 2 shows only one shared interface signal shared
between two peripherals, the sharing of interface signals

is extensible to multiple peripherals (as described above)
sharing multiple signals.

Referring now to **Figures 3A-3D**, a variety of
implementations of selection circuits in accordance with
various embodiments of the invention are shown. **Figure 3A**
shows an implementation of an output-only circuit wherein
the shared signal is an output to both peripheral A and
peripheral B. Two input signals (**In A** and **In B**) are
received by a selection circuit **30**, which includes two
tri-state buffers **32**. The tri-state buffer signals are
coupled to the chip select logic and the chip select logic
enables the appropriate tri-state buffer **32** corresponding
to the input signal required by a peripheral, prior to
selecting that peripheral by generating the peripheral
chip select signal. As described above, the selection is
made by an internal signal used to generate the chip
select signals, so that the appropriate tri-state buffer
32 will be enabled prior to the external chip select
enabling the selected peripheral integrated circuit and
stay enabled after the chip select signal disables the
selected peripheral integrated circuit. The maximum setup
time and the maximum hold time required among the set of
peripheral integrated circuits sharing a connection to an
interface pin determine the setup and hold time required
between the leading and trailing edge of the chip select
signals and the window in which the tri-state buffers are
enabled.

Figure 3B depicts an alternative embodiment of an
output-only selection circuit **40**. Selection circuit **40**
includes a multiplexer **42** coupled to the peripheral select
signal from the chip select logic for selecting between

signals **In A** and **In B**. Multiplexer **42** is coupled to an
output driver **44** for driving the appropriate selected
signal on a shared interface pin.

Figure 3C depicts a selection circuit **50** for sharing
a signal that is an output from one peripheral integrated
circuit and an input to a second peripheral integrated
circuit. A tri-state buffer **52** is used to isolate signal
In A from the shared output pin (**Out A / In B**) when
peripheral A is not selected. A transparent latch **56** may
be used to gate and hold a signal from the shared
interface pin by enabling transparent latch **56** when
peripheral B is selected (Similarly, an input-only
selection circuit may use two transparent latches to
implement this feature for two input signals).

Figure 3D depicts a selection circuit **60** for sharing
a pair of bi-directional signals. A transmission gate **62**
is used to isolate signal **Bi-Di A/B** to and from internal
node **Bi-Di A** when peripheral A is not selected. A second
transmission gate **64** is used to isolate **Bi-Di A/B** to and
from internal node **Bi-Di B** when peripheral B is not
selected. In the bi-directional signal sharing
implementations, the circuits coupled to internal node **Bi-Di A** and internal node **Bi-Di B** must not require input from
these nodes when the associated peripheral is not
selected, or additional signals providing information
regarding direction (output or input) on the shared pin
need to be accessible to the pin-sharing circuitry to
provide latching of input states when a bi-directional
signal is in an input state.

Referring now to **Figure 4**, signals within a system

controller integrated circuit in accordance with an
embodiment of the present invention are depicted in a
timing diagram. Prior to the assertion of chip select
signal **/CS1** (transition to logic low state), peripheral
select signal **SEL A/B** is in a logic high state, selecting
peripheral A. Peripheral A is selected for a setup time
T_{su} that is determined by the maximum setup time
requirements among the set of peripheral components
sharing an interface pin. While the specific timing
requirements of setup and hold time are particular to each
peripheral integrated circuit, for the purpose of design
simplicity, it is convenient to have a stable setup and
hold time common to the entire set of peripheral
integrated circuits sharing an interface pin or among the
peripherals sharing the entire set of interface pins. An
input signal **A** is valid before **/CS1** is asserted and is
coupled to the shared interface signal **Pin** and must meet
the setup time requirements for peripheral **A**, Similarly,
input signal **B** is valid before chip select signal **/CS2** is
asserted and **SEL A/B** selects peripheral **B** for interface to
shared interface signal **Pin**, causing input signal **B** to be
coupled to interface signal **Pin**. After de-assertion of
chip select signals **CS1** and **CS2** peripheral select signal
SEL A/B must remain valid for a hold time T_h that is
determined by the maximum hold time requirement among the
set of peripheral components sharing interface signal **Pin**.

While the invention has been particularly shown and
described with reference to the preferred embodiment
thereof, it will be understood by those skilled in the art
that the foregoing and other changes in form, and details
may be made therein without departing from the spirit and
scope of the invention.